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HYBRID MODEL OF THERMOSTABILIZATION OF THE DRAIN CURRENT IN *n*-CHANNEL MOS TRANSISTORS

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A hybrid model, which makes it possible to calculate the influence of the drain voltage and the temperature on the mobility of electrons in the n-channel of silicon MOS transistors with a high-alloy substrate in the linear regime of their operation on the basis of a combination of analytical approximations and modeling of electron transfer by the Monte Carlo method, has been proposed.

An important criterion of reliability of modern integrated submicron MOS (metal–oxide–semiconductor) transistors is their thermal stability. To obtain its numerical evaluation one currently uses different models which are based on the knowledge of the temperature gradients: the mobility of electrons in the conducting channel and the value of the threshold resistance in the range of variation of drain voltages much lower than the effective gate voltage [1]. Under the conditions of high concentrations of the impurity in the substrate, calculation of the values of these gradients turns out to be quite a difficult problem. Calculation of the mobility gradient is particularly difficult [1]. In this connection, it becomes pressing to develop models of such a kind that would enable one to quite adequately calculate the indicated quantities with the aim of optimizing the parameters of integrated MOS transistors. In the present work, we have proposed a hybrid model which makes it possible to evaluate the influence of a number of parameters on the electron mobility in the channel of an MOS transistor with a high concentration of the acceptor impurity.

To substantiate and analyze this model we carried out experimental measurements of test transistors manufactured according to the standard technology of integrated circuits on a *p*-type silicon substrate. Figure 1 gives experimental volt-ampere characteristics measured at different temperatures of the test MOS transistor with the parameters $N_a = 7 \cdot 10^{23}$ m^{-3}, $L = 4$ μm, $W = 24$ μm, $x_{ox} = 0.3$ μm, $x_j \approx 0.5$ μm, and $V_g = 70$ V. The volt-ampere characteristics calculated using the model developed in the present work are shown dashed in this figure. The drain current in the saturation regime was set constant according to [2]. It is easily seen that, when the temperatures are low, the agreement between the experimental and calculated curves is good.

According to Fig. 1, transition to the saturation of the drain current on the volt-ampere characteristics of the transistors under study occurs at drain voltages lower in value than the doubled potential in the neutral silicon volume (for the transistor under study we have $2\varphi_f \approx 1$ V). Therefore, in calculating the drain current, we can use the equation obtained according to the existing procedure of a variable charge of the depletion region of the silicon substrate in the range of variation of the voltage $V_d < 2\varphi_f$ [3]:

$$I_d = \mu C_0 \frac{W}{L} \left[(V_g - V_t)\, V_d - b_0 V_d^2 \right] , \tag{1}$$

where the electron mobility is assumed to be constant along the channel and the parameter b_0 corresponds to the relation

$$b_0 = \frac{1}{2} + \frac{a_0 f}{3\sqrt{2\varphi_f + V_{sb}}} , \quad a_0 = \sqrt{2\varepsilon_s e N_a}/C_0 , \quad f = 1 - \frac{x_j}{L}\left(\sqrt{1 + \frac{2x_{d.m}}{x_j}} - 1\right), \quad \varphi_f = \left(\frac{kT}{e}\right) \ln \frac{N_a}{n_i} . \tag{2}$$

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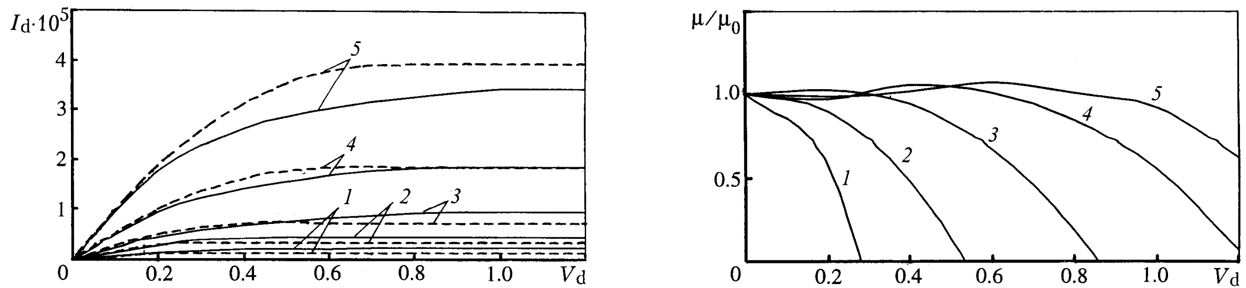

Fig. 1. Experimental (solid) and calculated (dashed) curves of the volt-ampere characteristic of an MOS transistor under investigation: 1) T = −110°C and V_t = 60 V, 2) –20 and 45, 3) +20 and 38; 4) +60 and 30, and 5) +100 and 25. I_d, A; V_d, V.

Fig. 2. Dependence of the ratio of the electron mobility at $V_d < 2\varphi_f + V_{sb}$ to the electron mobility at $V_d \to 0$ on V_d; 1–5 are obtained for the same values of T and V_t as the analogous curves in Fig. 1. V_d, V.

The proposed algorithm of calculation of the mobility under the conditions of high concentrations N_a within the framework of the model developed is based on determination of the relation between the current and the mobility in weak fields, on the one hand, and the current and the mobility in stronger fields, on the other. For the current I_0 corresponding to a constant mobility of the electrons in a weak field

$$\mu_0 = \left[\left(\frac{dI_d}{dV_d}\right)_{V_d \to 0}\right] \frac{L}{C_0 (V_g - V_t) W},$$

we find from (1) the mobility relation [3]

$$\frac{\mu_0}{\mu} = \frac{I_0}{I_d}\left(1 - b_0 \frac{V_d}{V_g - V_t}\right). \tag{3}$$

The deviation of the ratio μ_0/μ from unity with increase in V_d in the range 0–2φ_f characterizes the influence of the longitudinal field produced by the drain voltage on the mobility μ. The decrease in the current I_d, which can be due to the drop in μ as the drain voltage increases, suppression of the inversion conductance near the drain junction, spreading of the streamlines deep into the substrate, and increase in the resistance of the depletion region of the backward-biased n^+–p drain junction, will partially be compensated for with a decrease in the multiplier in the parentheses of (3). The value of this multiplier is determined by the coefficient b_0, which depends on the form of expansion, in a binomials series, of the expression for the drain current, obtained with allowance for the variable charge of ionized impurity atoms in the depletion region of the substrate and for the presence of the inversion layer throughout the length of the conducting channel [3–5]. The value of the coefficient b_0, calculated according to [3], exceeds the value of b_0 in [4, 6], which enables us to disregard the influence of the longitudinal electric field on the electron mobility in the prescribed range of variation $V_d < 2\varphi_f + V_{sb}$ in identifying the experimental and calculated volt-ampere characteristics. Figure 2 shows the dependences of μ/μ_0 on V_d of the test transistor, which have been calculated at different temperatures and V_g = const. As is clear from the figure, a temperature change exerts no appreciable influence on the behavior of the curves obtained from (3) in the range of variation of the drain voltage $0 < V_d < 2\varphi_f$.

Figure 3 gives the relative values μ/μ_{-110} of the electron mobility in a weak longitudinal field at different temperatures of the transistor (curve 1). For the sake of comparison, this figure also gives results of modeling of the mobility of electrons (curve 2) in their transfer in the n channel of a silicon MOS transistor by the Monte Carlo method in accordance with the algorithm of [7]. Analyzing the kinetics of drift of the electrons, which is successively tracked in modeling by the Monte Carlo method from the previous act of scattering to the next act, we can explain the extremum of the dependence of μ/μ_{-110}, observed in the region of temperatures T = 10–20°C, by the complex temperature character of screening of the Coulomb potential of scattering on impurity ions. At the temperature

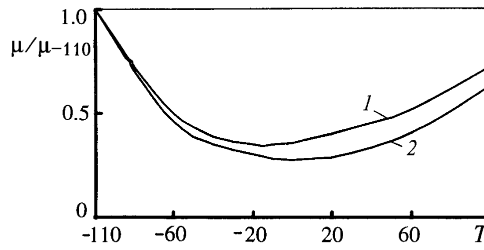

Fig. 3. Calculated dependence of the ratio of the mobility at different temperatures to the mobility at $T = -110^{\text{o}}$C (1) and the dependence obtained by numerical modeling of carrier transfer according to the Monte Carlo method (2).

$T \approx 20^{\text{o}}$C, we have maximization of the intensity of both the scattering on impurity ions and the phonon scattering, whereas in other temperature regimes we observe a significant decrease in the intensity of either one mechanism of scattering or the other: the phonon scattering at low temperatures and the impurity scattering at high temperatures.

Let us consider the algorithm of calculation of the thermostability point in accordance with the adopted approximations. Taking the logarithm of (1) and then differentiating it with respect to temperature, we obtain

$$\frac{1}{I_{\text{d}}}\frac{dI_{\text{d}}}{dT} = \frac{1}{\mu}\frac{d\mu}{dT} - \frac{1}{V_{\text{g}} - V_{\text{t}} - b_0 V_{\text{d}}}\left(\frac{dV_{\text{t}}}{dT} + \frac{db_0}{dT}V_{\text{d}}\right), \tag{4}$$

where $V_{\text{t}} = 2\varphi_{\text{f}} + V_{\text{f.b}} + Q_{\text{a}}/C_0$. The threshold voltage has been determined on the source junction. The thermostable point on the volt-ampere characteristic $I_{\text{d}} = f(V_{\text{g}})$ at which the drain current and the gate voltage are constant at different chip temperatures is characterized by equality of the right-hand side of (4) to zero [1]. Employing this condition, we obtain from (4) an expression for calculating the effective gate voltage $(V_{\text{g}} - V_{\text{t}})$ at which we can have thermostabilization of the current in the transistor channel:

$$V_{\text{g}} - V_{\text{t}} = \mu \frac{\dfrac{dV_{\text{t}}}{dT} + \dfrac{db_0}{dT}V_{\text{d}}}{\dfrac{d\mu}{dT}} + b_0 V_{\text{d}}\,. \tag{5}$$

As follows from (5), with increase in the voltage V_{d} the thermostable point on the volt-ampere characteristic can shift to the region of higher voltages $(V_{\text{g}} - V_{\text{t}})$. The first term on the right-hand side of (5) will be determined by the value and signs of the gradients dV_{t}/dT and db_0/dT and by the multiplier $\mu/(d\mu/dT)$. For $dV_{\text{t}}/dT < 0$, $dV_{\text{t}}/dT > V_{\text{d}}(db_0/dT)$, and $d\mu/dT < 0$ [8], the sign of this term will be positive, which causes a growth in the effective gate voltage in thermostabilization. In the test high-alloy transistor considered in this work, $b_0 \approx 20$, the sign of the gradient $d\mu/dT$ changes with increase in the temperature (Fig. 3), and the thermostable point can shift to the region of lower gate voltages. In [9], $dV_{\text{t}}/dT \approx 7 \cdot 10^{-4}$ V/K, $b_0 \approx 0.6$, $N_{\text{a}} = 3.6 \cdot 10^{23}$ m^{-3}, and the second term on the right-hand side of (5) is comparable with a change in V_{t} in the prescribed range of temperatures (290–420 K), which makes it necessary to allow for the influence of the drain voltage on the thermostability of the transistor.

As the temperature of the device increases, the drain current increases and the current-saturation voltage $V_{\text{d.s}}$ shifts to the region of higher values of V_{d} (Fig. 1). It follows from (1) that the extremum of the current (it corresponds to the condition $dI_{\text{d}}/dV_{\text{d}} = 0$) is attained at the voltage

$$V_{\text{d}} = V_{\text{d.ex}} = \frac{V_{\text{g}} - V_{\text{t}}}{2b_0}\,. \tag{6}$$

If the condition $V_{\text{d.ex}} = V_{\text{d.s}}$ holds on transition to saturation, the above formula (6) enables us to determine this voltage. In the temperature range considered with allowance for the change in V_{t} and the fraction of ionized impurity atoms in the transistor substrate the voltage $V_{\text{d.ex}}$ is 0.2–1.5 V, which is in agreement with the measured values (see

Fig. 1). The growth in the drain current with temperature (Fig. 1) is attributable to the more appreciable influence of the dependence $V_t(T)$ on the value of this current as compared to the influence of the dependence $\mu(T)$ [1].

Thus, we have proposed a hybrid model making it possible, in combination with certain approximations and approaches, in particular, the kinetic modeling of electron transfer by the Monte Carlo method, to quite adequately study the influence of a number of external factors and structural parameters on the parameters of thermostabilization of high-alloy *n*-channel MOS transistors.

NOTATION

N_a, concentration of acceptors in the substrate, m^{-3}; L and W, length and width of the transistor channel, μm; x_{ox}, thickness of the subgate oxide, μm; x_j, depth of occurrence of the source and drain regions, μm; μ, mobility of electrons in the channel, $m^2/(V\cdot sec)$; C_0, specific capacitance of the oxide, F/m^2; V_g, gate voltage, V; V_d, drain voltage, V; V_t, threshold voltage of the device, V; ε_s, dielectric constant, F/m; e, electron charge, C; kT/e, thermal potential, V; T, temperature, K; k, Boltzmann constant, J/K; n_i, intrinsic concentration of the charge carriers, m^{-3}; V_{sb}, voltage applied to the substrate, V; $x_{d.m}$, depth of the depletion substrate region in the regime of strong inversion, μm; φ_f, potential in the neutral silicon volume, V; I_d, drain current of the transistor, A; μ_{-110}, mobility of electrons in the channel at the temperature $T = -110^oC$, $m^2/(V\cdot sec)$; $V_{f.b}$, flat-band voltage, V; Q_a, surface density of ionized impurity atoms, C; $V_{d.ex}$, drain voltage at which the drain current is maximum, V. Subscripts: a, acceptor; ox, oxide; j, junction; g, gate; d, drain; t, threshold; s, semiconductor; i, intrinsic; sb, substrate; d.m, maximum of the depletion region; f, reduced Fermi level; f.b, flat bands; d.ex, drain extremum; d.s, drain saturation.

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